Conventional Vertical Power MOSFET Device Structure

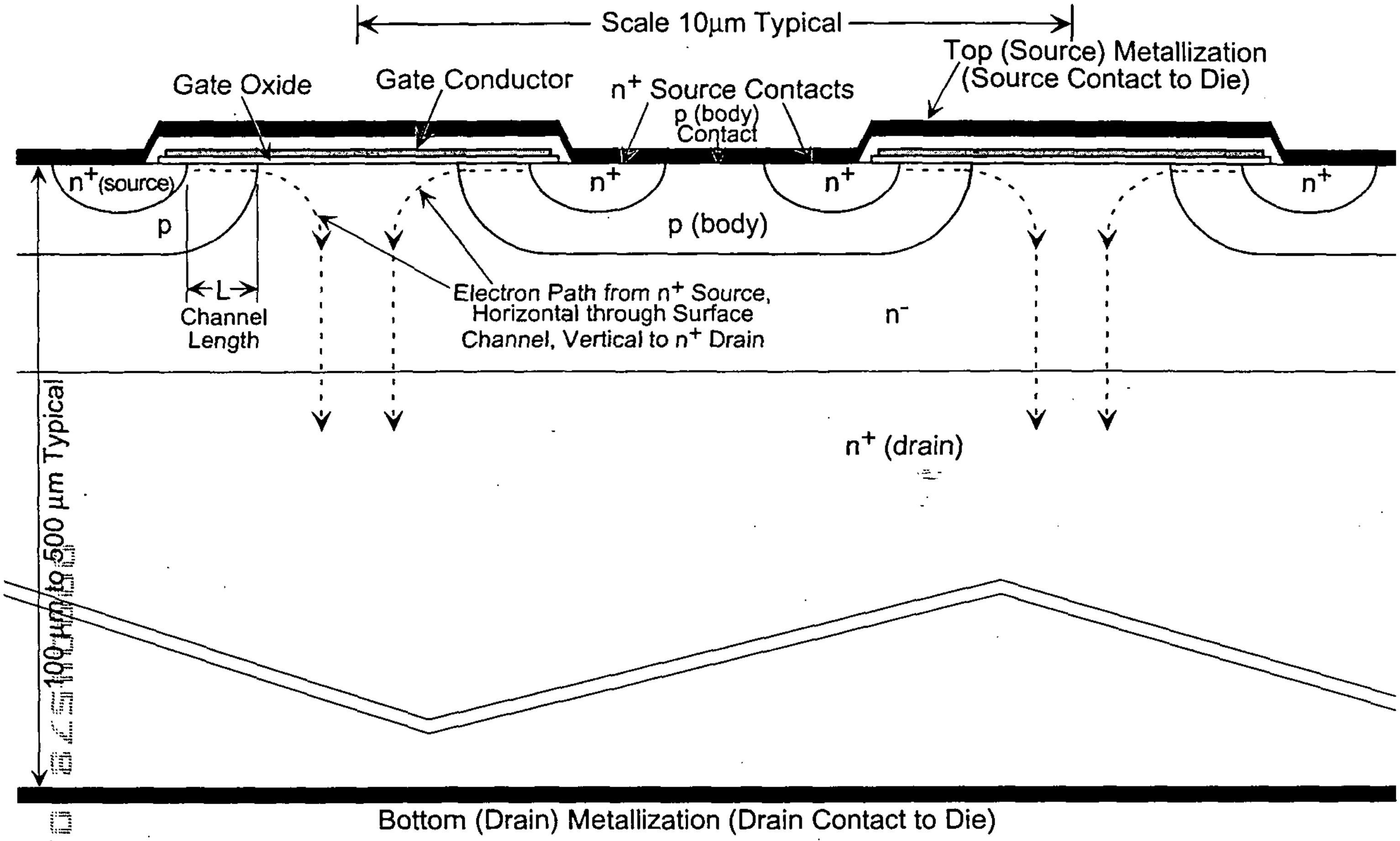

FIG. 1A

CMOS-Implemented Planar Geometry High Current Switching MOSFET Device Structure

Scale 2.0µm Typical

Note: Only M1(1st metal layer) shown; collection of all of the Source, Drain and Gate electrodes into High-Current Source and Drain Chip Contacts on M5 is accomplished in metal layers M2-M5.

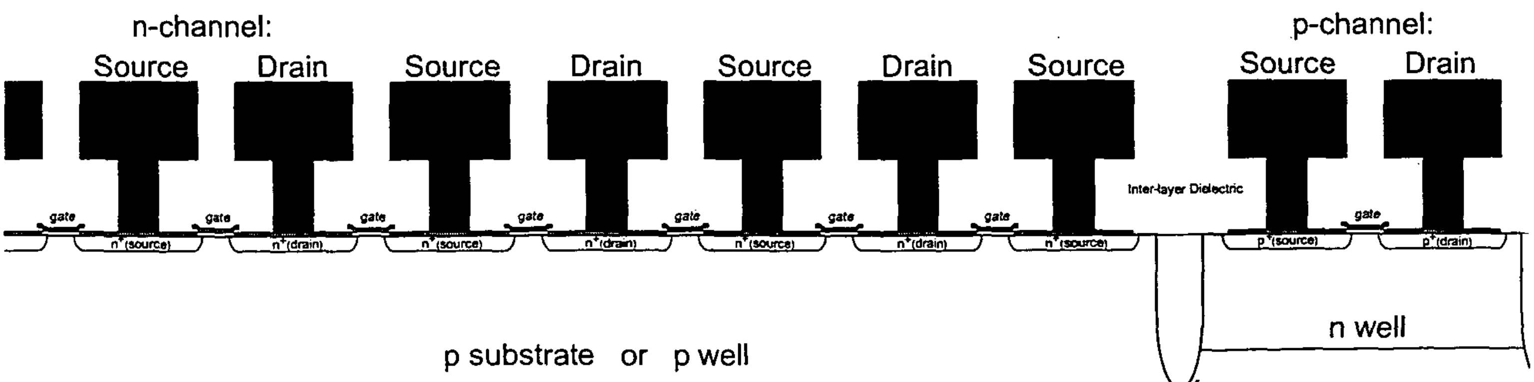

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FIG. 1B

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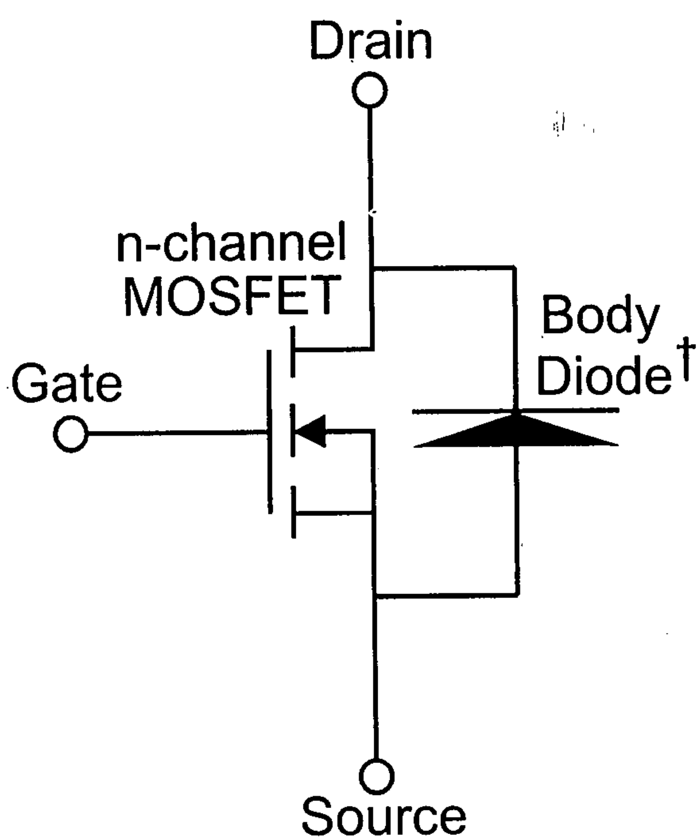
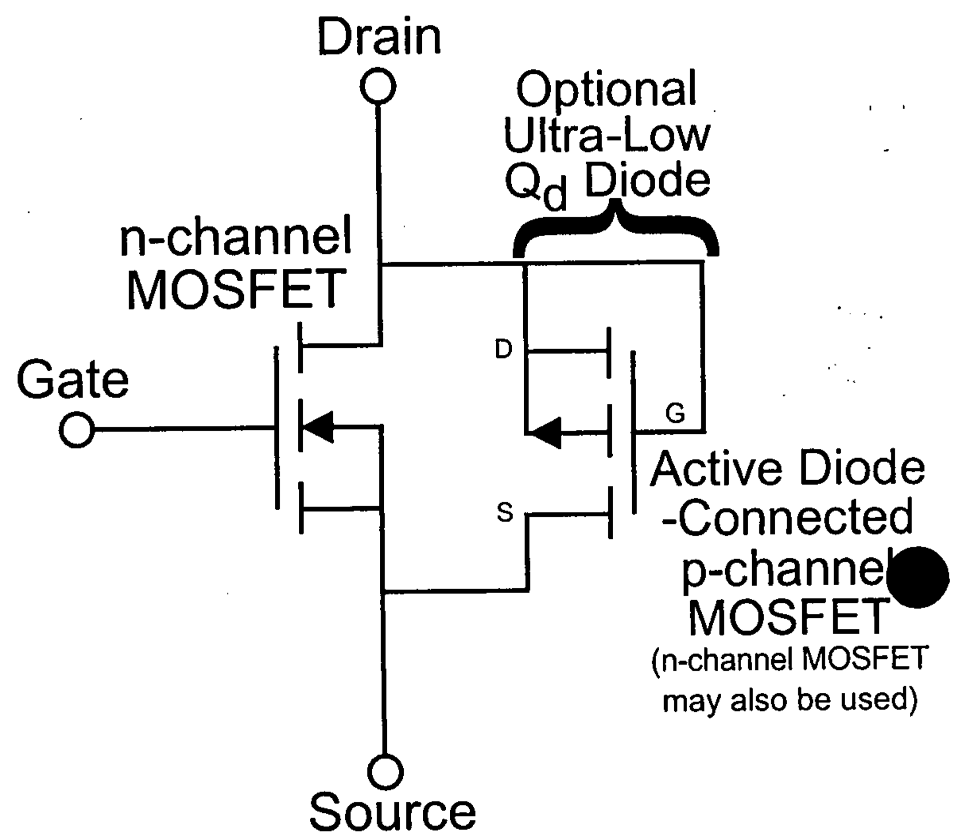
Conventional Power MOSFET Equivalent Circuit



†Note that Body Diode is a very large area p-n^--n^+ diode with a very large diffusion charge storage capacity, Q_d. This means that when the body diode is first reverse biased after heavy forward conduction, a large transient reverse current, I_r, can flow for a substantial period of time, $t_r=Q_d/I_r$, which can limit usable switching frequencies.

FIG. 2A

CMOS-Implemented High Current MOSFET Equivalent Circuit



While a p-channel MOSFET with gate connected to Drain is illustrated, an n-channel MOSFET with its gate connected to the Source electrode will also serve as the active "body diode", turning on when the Drain electrode becomes more negative than the Source electrode by an amount greater than the threshold voltage, V_t, of the MOSFET. Note that if the Gate of the switching MOSFET is constrained to go no more negative than the Source, then it will, by itself, act as the "body diode".

FIG. 2B

Cross-Section of 200 amp Planar Switching MOSFET Chip and Part of Package

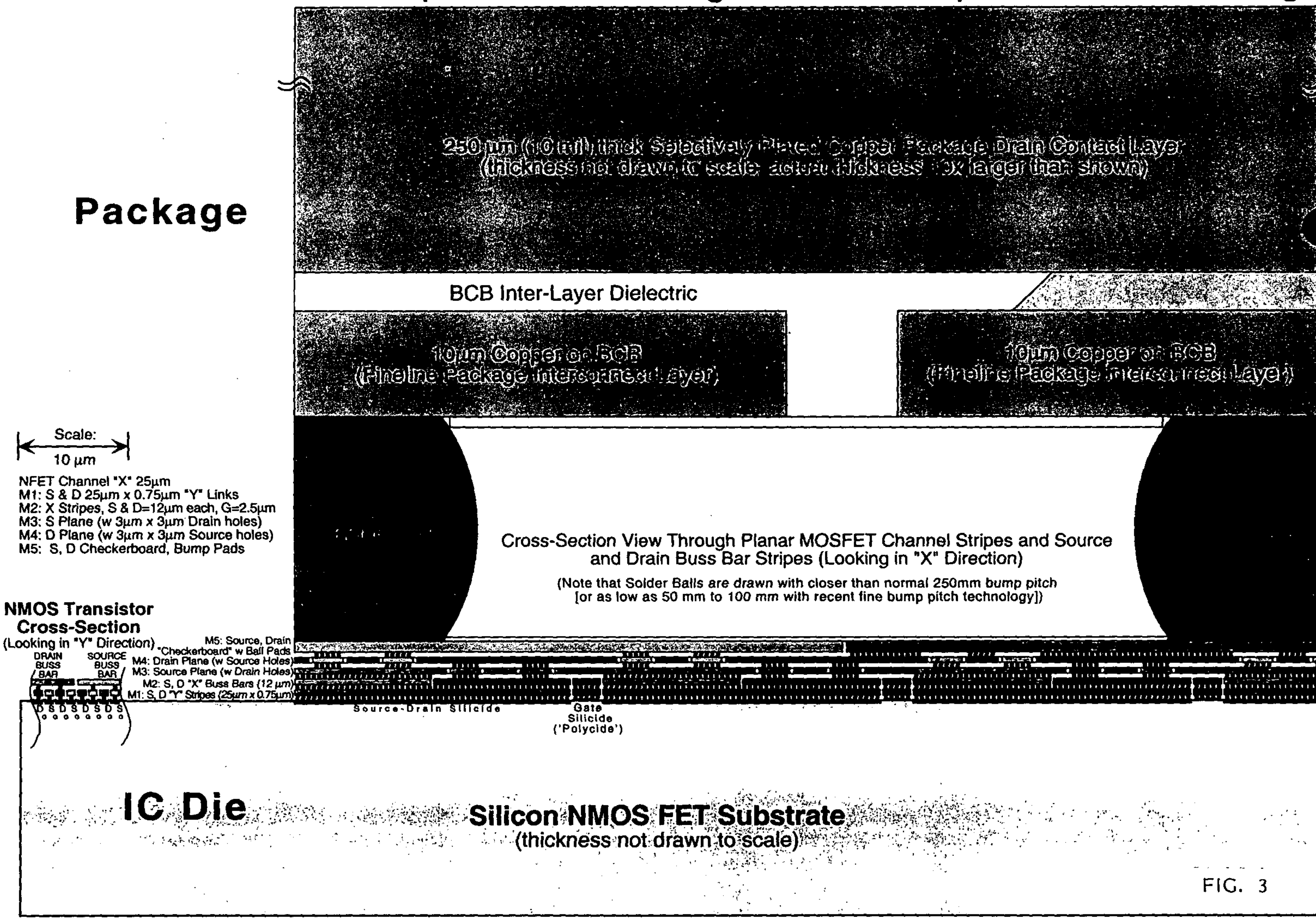


FIG. 3

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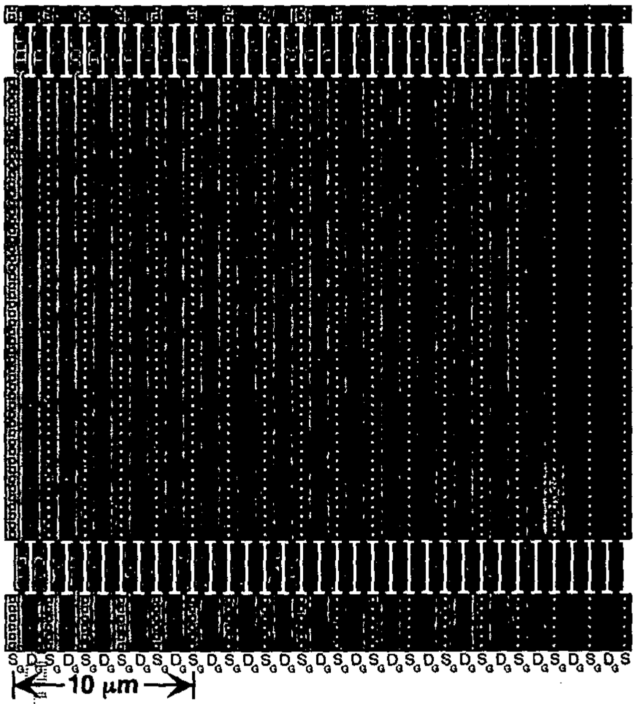
200 amp NMOS Switching FET Chip; Mask Levels M1-M3 & Poly

FIG. 4A

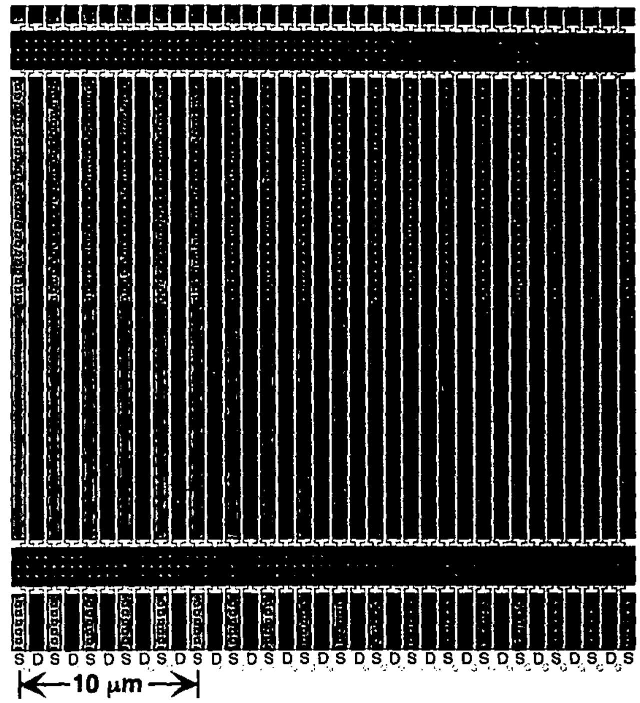
Sourc (Red)/Drain (Blue) Polysilicide and Gate (Gr en) Polysilicid with Vias to Metal 1



One complete 25µm high row of NMOS FET channel, with portion of rows above and below, is shown. Each row completes W≈250µm of NFET width in 10µm horizontal distance. S/D ohmic contact polysilicide (4Ω/Sq) shown in red for sources, blue for drains, with vias to Metal 1 (7.5Ω/cut) used to reduce current path resistance. Gate polysilicide (7Ω/Sq) is shown in green, with vias to M1 between rows.

FIG. 4B

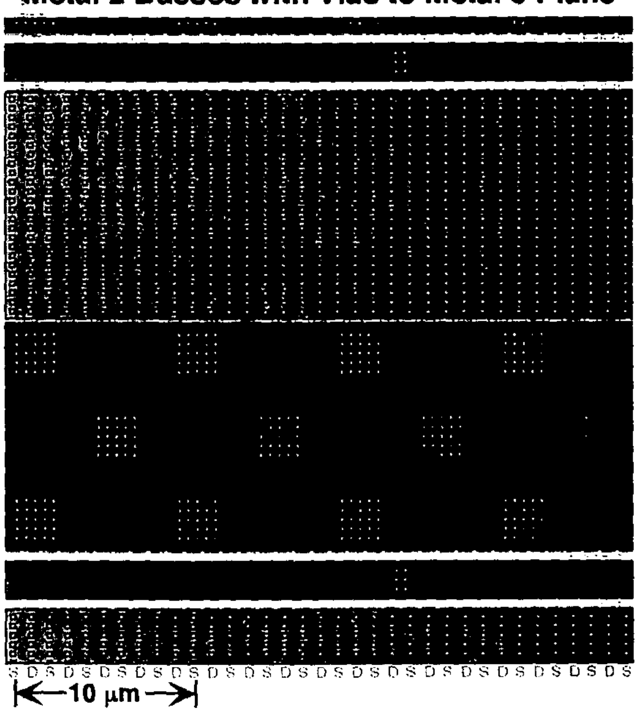
Source (Red), Drain (Blu) and Gat (Green) Metal 1 Jumpers with Vias t Metal 2 Bu ses



Metal 1 (M1; 0.08Ω/Sq) source and drain straps, 0.75µm x 25µm, are used to reduce resistance of S/D polysilicide in passing current to M2 horizontal S and D busses. Since source M2 buss is taken to cover the upper half of the 25µm channel, the source stripes (red) carry the current from the lower half of the channel to the M1 to M2 vias (5Ω/cut) on the upper half of the channel, and visa-versa for the drain stripes (blue).

FIG. 4C

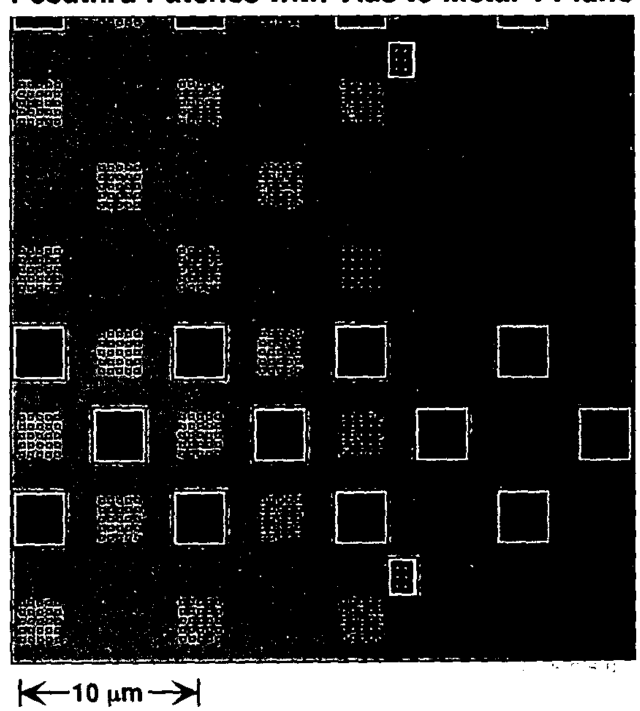
Sourc (Red), Drain (Blue) and Gate (Green) Metal 2 Busses with Vias to Metal 3 Plane



Horizontal source (red) and drain (blue) M2 (0.08Ω/Sq) busses tie the M1 source and drain stripes together. Since the next, M3, layer is a source plane, the source buss is completely covered with M2/M3 vias (5Ω/cut). The connections from the M2 drain busses to the M4 drain plane are done through an array of isolated M3 patches in the M3 source plane, so the drain buss M2/M3 vias are in patches as shown.

FIG. 4D

Source Metal 3 Plane (Red) & (Blu) Drain M3 Feedthru Patches with Vias to Metal 4 Plane



Metal 3 (0.08Ω/Sq) source plane (red) with isolated drain feedthru pads (blue) with M3/M4 via patches carrying current from the M2 drain busses to M4 drain plane. Left 22µm in area shown is under source M5 'checkerboard' pad contact area, so source plane has array of M3/M4 via patches going to isolated feedthru's in M4 drain plane. Right 13µm of area shown has drain M5, so here M3 carries source current laterally

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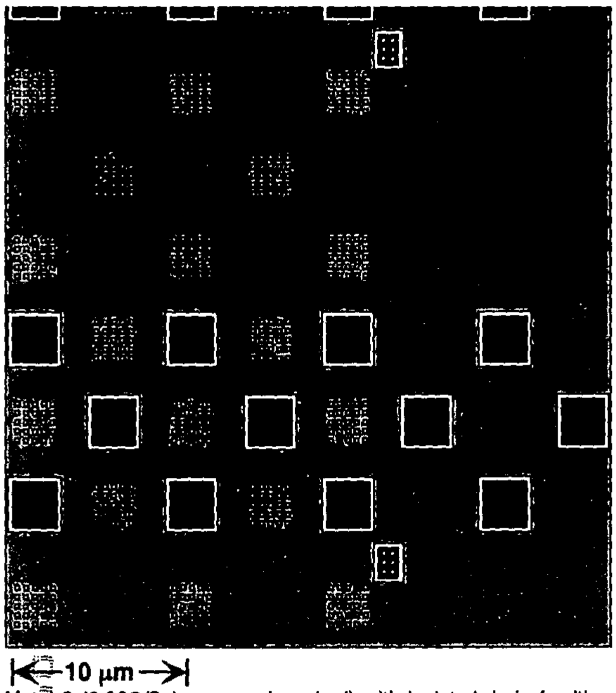
200 amp NMOS S itching FET Chip: Ma k Levels M3-M5 & Ball

FIG. 5A

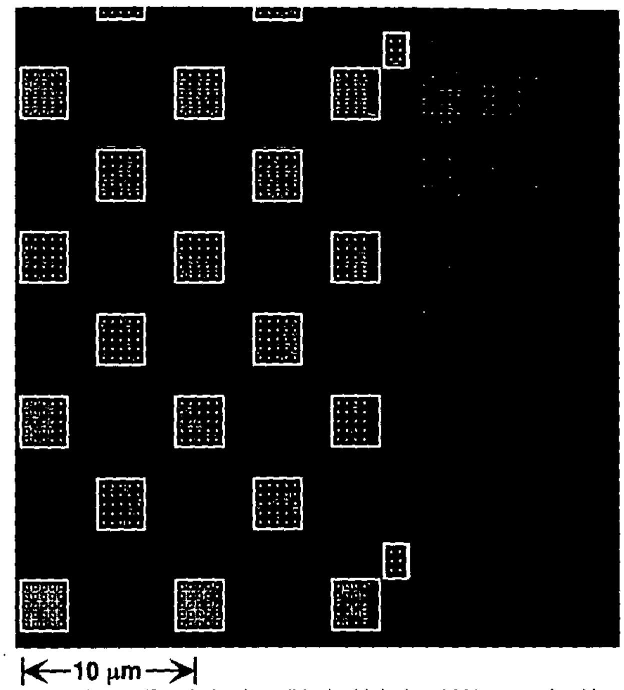
Sourc Metal 3 Plan (Red) & (Blu) Drain M3 Fe dthru Patches with Vias to M tal 4 Plane



Metal 3 (0.08Ω/Sq) source plane (red) with isolated drain feedthru pads (blue) with M3/M4 via patches carrying current from the M2 drain busses to M4 drain plane. Left 22μm in area shown is under source M5 'checkerboard' pad contact area, so source plane has array of M3/M4 via patches going to isolated feedthru's in M4 drain plane. Right 13μm of area shown has drain M5, so here M3 carries source current laterally.

FIG. 5B

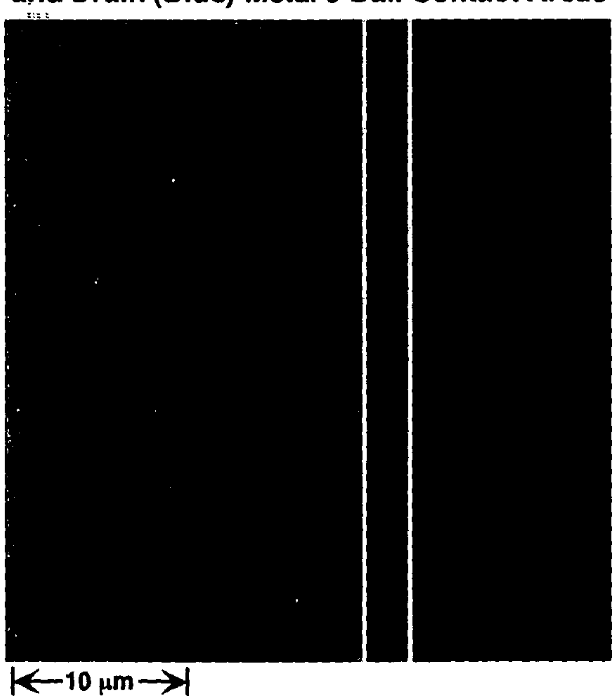
Drain M tal 4 Plan (Blue) & (Red) Source M4 F edthru Patch s w Vias to Metal 5 Contacts



Metal 4 (0.08Ω/Sq) drain plane (blue) with isolated M4 source feedthru pads (red) with M4/M5 via patches carrying current from the M3 source plane to M5 source 'checkerboard' pad contact area over left 22μm of area drawn. Since right 13μm of area shown has drain M5, this area is covered with M4/M5 vias connecting M4 drain plane with M5 drain pads.

FIG. 5C

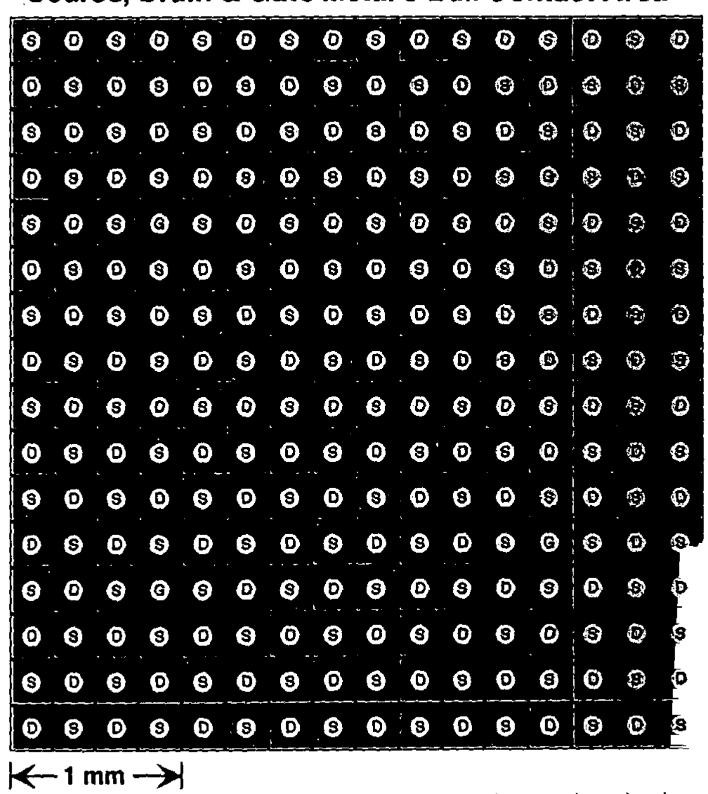
Detail of Part of 'Checkerboard' Source (Red) and Drain (Blue) Metal 5 Ball Contact Areas



Small area of Metal 5 (0.04Ω/Sq) ball contact pad 'checkerboard' to same scale as previous drawings. Red area covering left 22μm of drawing is the right side of a source M5 ball contact pad, while the blue area (right 13μm) is the left side of a drain M5 pad. These M5 ball contact pads are nominally 250μm square using standard flip-chip ball pitches, or 100μm or less using advanced 'SHOCC' ball pitches.

FIG. 5D

Full Chip View of Solder Balls and 'Checkerboard' Source, Drain & Gate Metal 5 Ball Contact Area



Full chip view of 4mm x 4mm die (scale 100x larger than previous drawing showing Metal 5 (0.04Ω/Sq) source (red), drain (blue) and gate (gree 'checkerboard' of ball contact pads with solder balls at their centers. While 250μm flip-chip ball pitch is shown, reducing to ≤100μm would improve metal resistance

FIG. 6A

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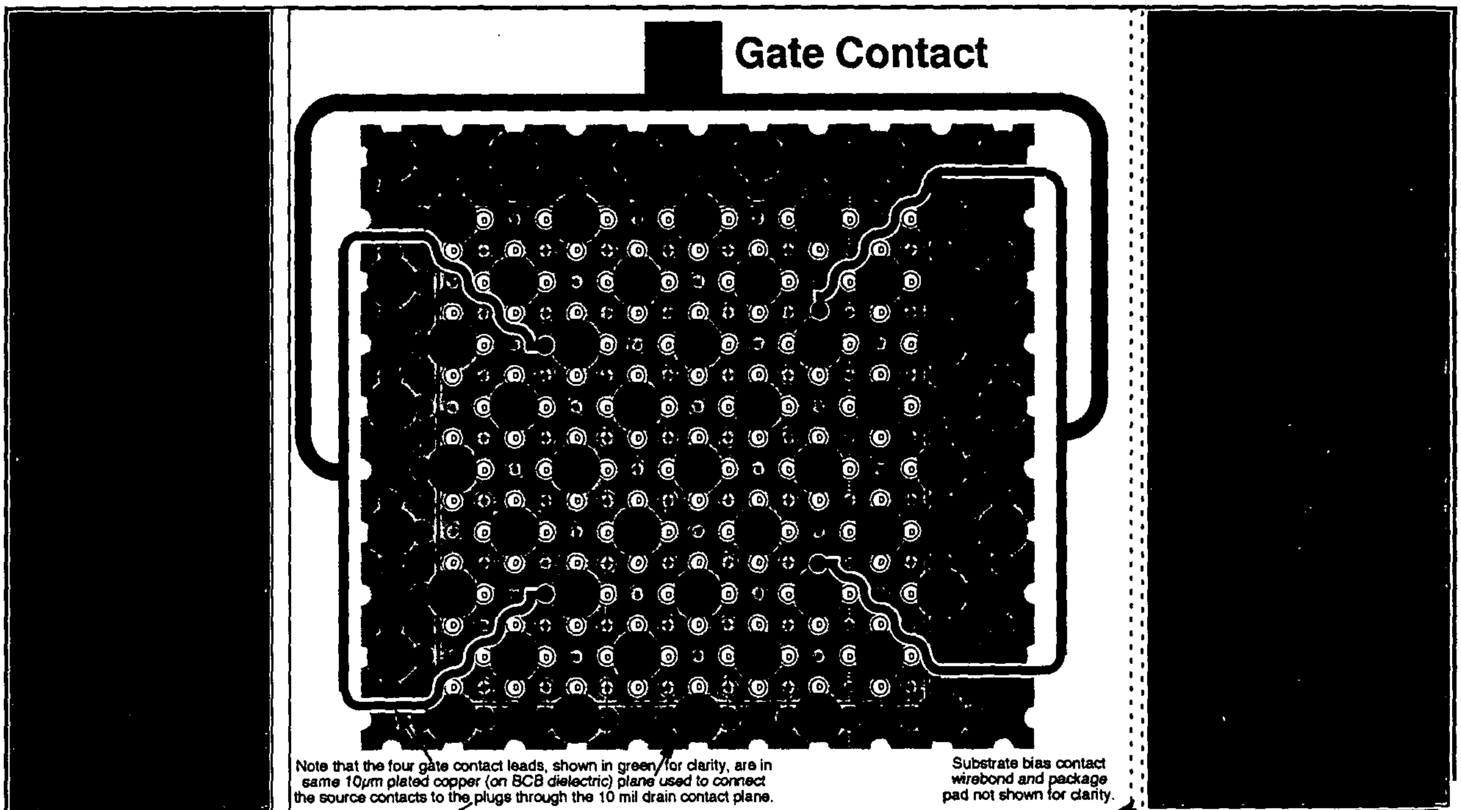

FIG. 6B

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Cross-Section of 200 Amp Planar Switching MOSFET Chip After Full-Wafer Deposition of Additive Copper/Polymer Interconnect Layers on Completed IC Wafer

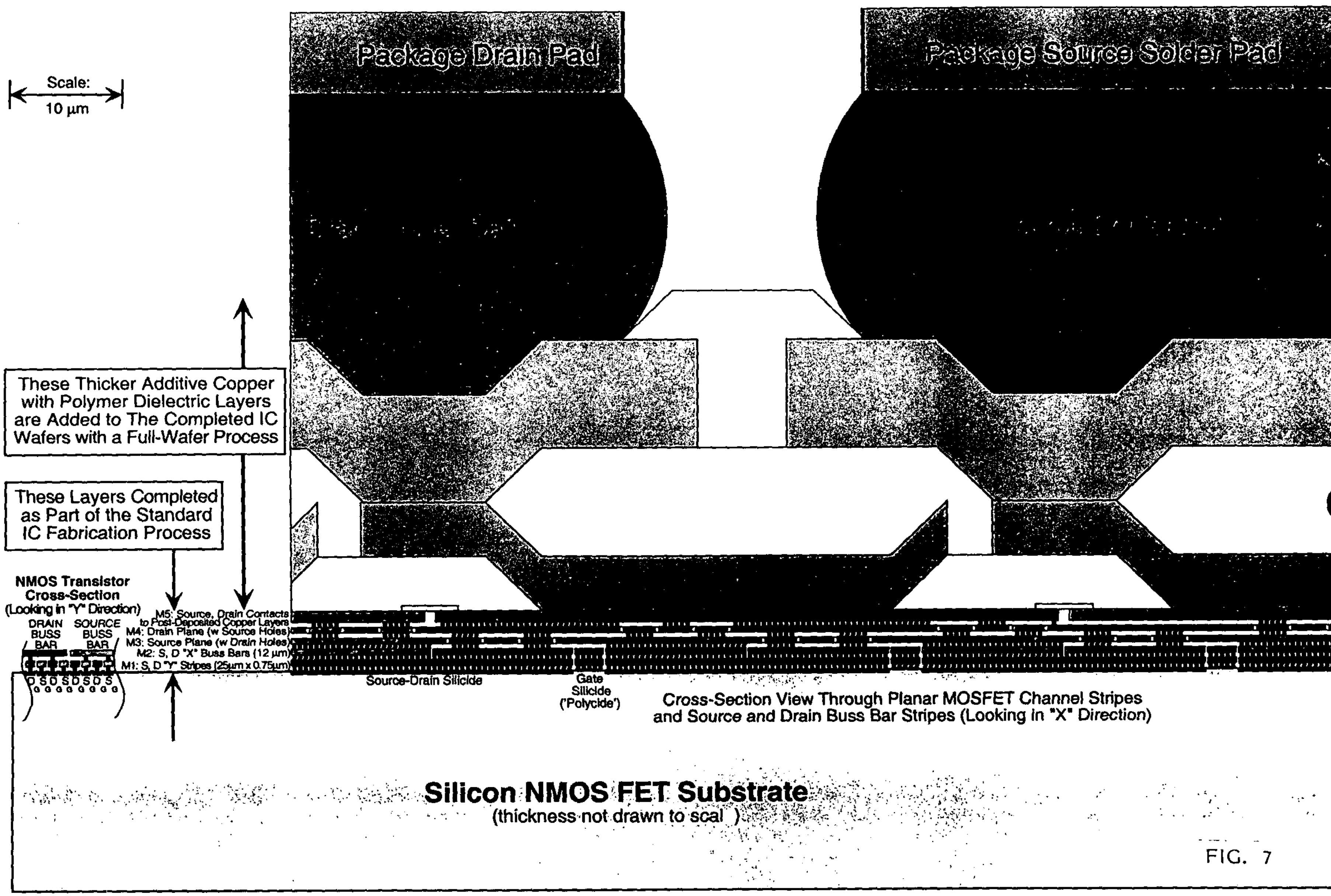


FIG. 7

R.C. Eden 7/31/00

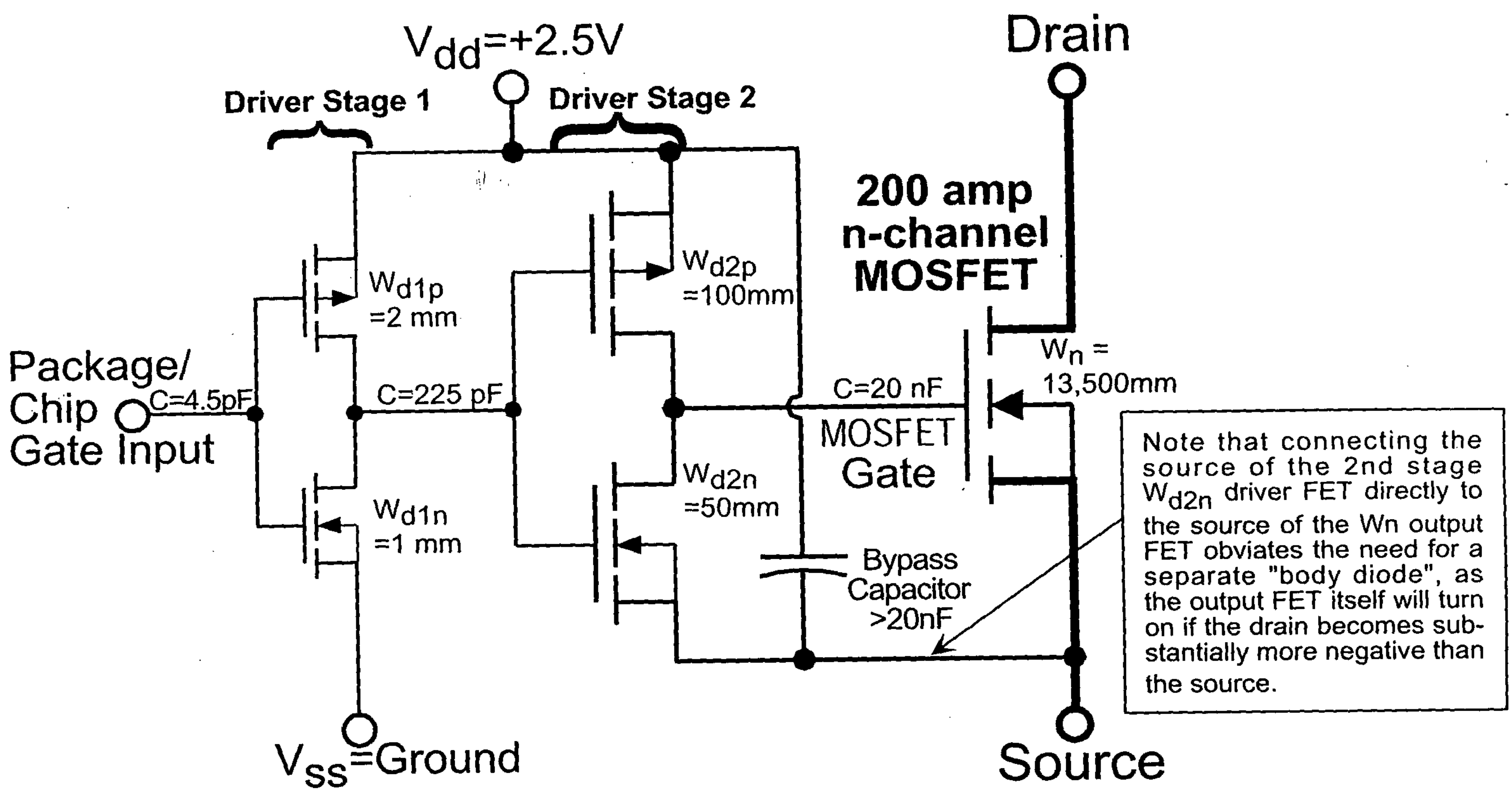


FIG. 8

R. C. Eden 10/8/00

Alternate "Stripe" Layout of 200 amp NMOS Switching FET Chip with Gate Drive Amplifier for Compatibility with Very Low Resistance Vertically Laminated Package

Full Chip View of Sold r Balls and Source, Drain & Gate Metal 5 Ball Contact Areas

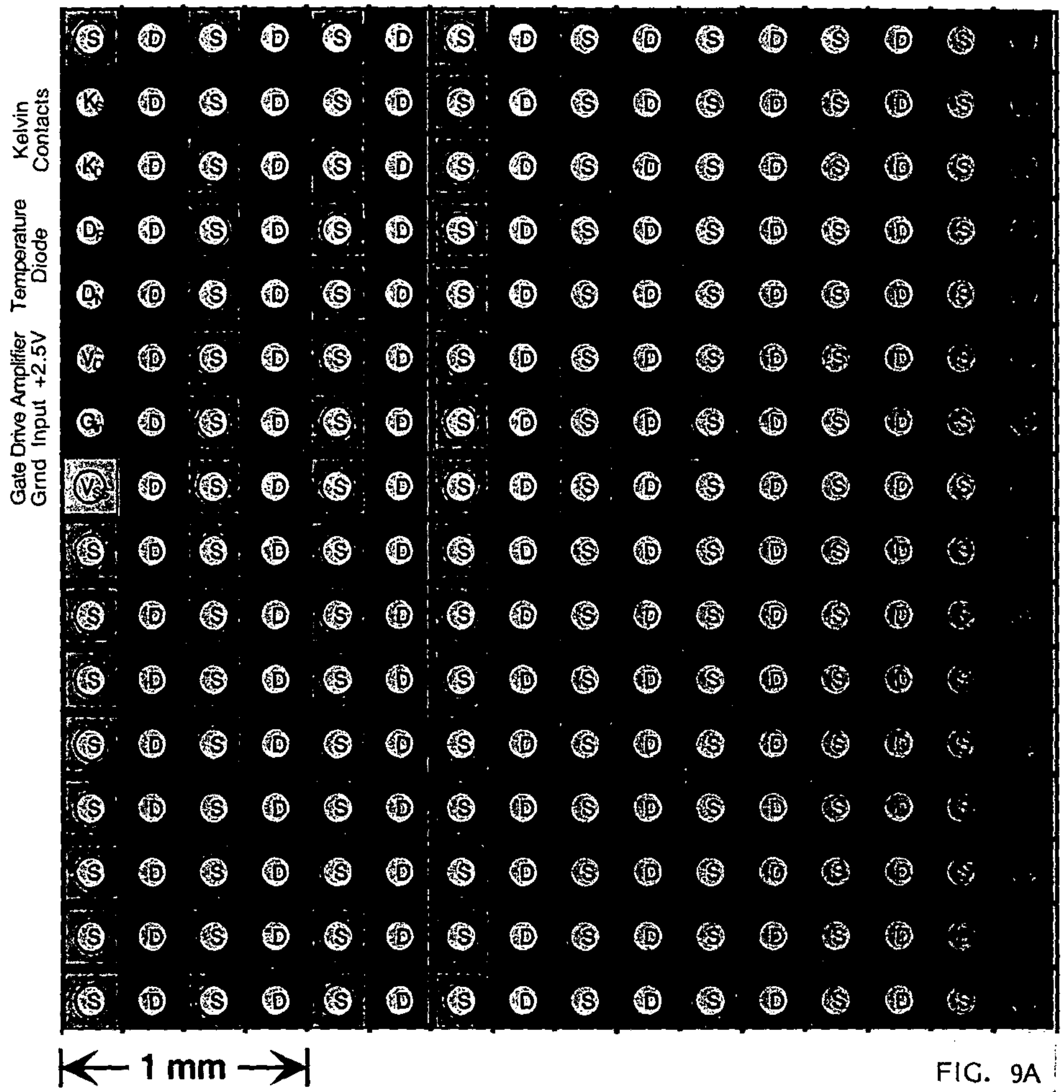
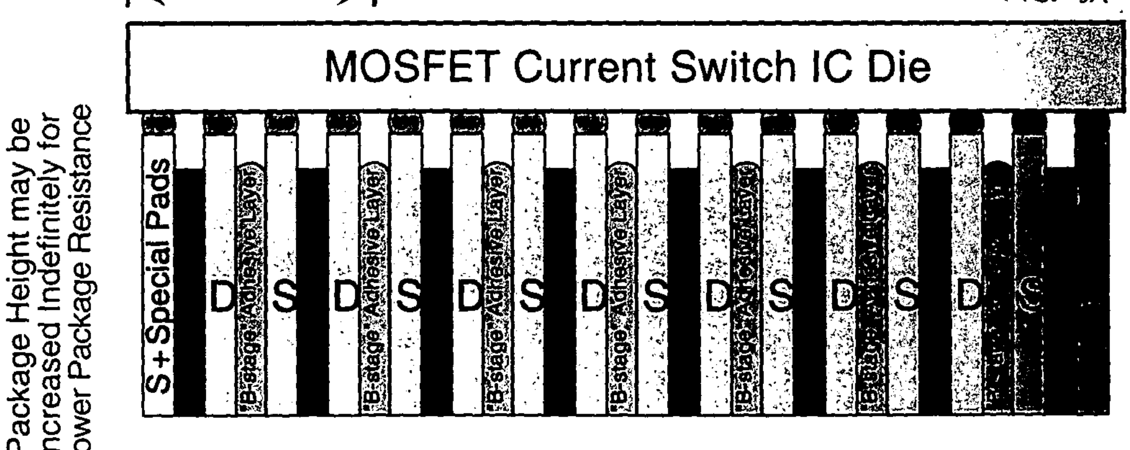


FIG. 9A



Side View of Mating Very Low-R Vertical Laminate Package

FIG. 9B

<u>250µm Bump Pitch</u> Calculation of 0.19µm Power Switching FET Resistance with On-Chip Metal and Package R

Richard C. Eden 9/14/99

NFET Channel X 25µm M1: S & D 25µmx1µm Y Links M2: X Stripes, S & D=24µm each, G=2.5µm M3: S Plane (w 5x15 D h's) M4: D Plane (w S h's) M5: S, D Pad Checkerboard

Total Channel W=	12.5	meters	12500000	µm	
Lambda (Lgd/2)=			0.125	µm	
Source/D Width=	6	Lambda	0.75	µm	
Source/D Stripe=			25	µm	
Gate Stripe W=			3	µm	
Vertical Pitch Py=			28	µm	
Horizontal Pitch Px=			2	µm	
FET Ch W in Pitch Wp=			50	µm	
Nominal FET Die Area=	14	mm^2	14000000	(µm)^2	
Square Die Size=	3.74166	mm	3741.6574	µm	
Drain Via Patch x=			2.5	µm	
D Via Patch Pitch Xp=			5	µm	
Drain Via Patch y=			2.5	µm	
# of Vias per Patch=			25	Vias/Patch	
Sheet R for M1-M4			0.08	Ω/Sq	0.5 µm Aluminum
Sheet R for M5			0.04	Ω/Sq	1.0µm Aluminum
Solder Ball Resistivity	2.2E-05	Ω-cm	22	µΩ-cm	
Solder Ball Sheet R	0.00293	Ω/Sq	0.0029333	Ω/Sq	Thickness=0.3 ball pitch
Actual Chip Size=	4	mm			
Ball Pitch=	0.25	mm	250	µm	
Number Balls on Chip	16	Balls/Row	256	Balls/chip	
Equiv M5 R2/R1 ratio			2		
Equiv Ball R2/R1 ratio			2		
Copper Resistivity	1.7E-06	Ω-cm	1.7	µΩ-cm	
Number Cu/BCB Layers			1	Layer(s)	
Cu on BCB Thickness	0.001	cm	10	µm	
Cu on BCB Sheet R	0.0017	Ω/Square	1.7	mΩ/Sq	
Thick Plated Cu Tm	0.0254	cm	10	mils	
Thick Plated Cu Sheet F	6.7E-05	Ω/Square	0.0669291	mΩ/Sq	
Source Via Plug Dia	0.01524	cm	6	mils	
Diagonal Plug Pitch	0.70711	mm	17.960512	mils	
Total Package Length	1.25	cm	0.492126	inches	
Effective Plane Lpe=	0.5	cm	5	mm	2/3 of chip to far contact pad+0.75mm
Package Width, Wp=	0.8	cm	0.3149606	inches	
Cu-Invar-Cu Substr Tm	0.0508	cm	20	mils	
Cu-Invar-Cu Sheet R	3.3E-05	Ω/Square	0.0334646	mΩ/Sq	

DC Resistance Results Summary:

	Source µΩ	Drain µΩ	Total S+D µΩ		
Silicon/Translator:	38.40	38.40	76.80		76.8
On-Chip Metallization:	50.49	51.96	102.44		102.43982
Package Metal:	65.53	52.33	117.86		117.86174
Total Si+Metal+Package Resistance:	154.41	142.69	297.10	Micro-Ohms	297.10156
200 Amp 50% DC Power (W)=	3.088	2.854	5.942	Watts	
			2.48%	Loss at Vout=1.2V	

Calculated for Package Conditions:			
Ball Pitch (µm)=	250		
Number of Copper/BCB Layers=	1	Thickness (µm)=	10
Thick Plated Cu Drain Plane Tm(mils)=	10	or Tm(µm)=	254
Via Stud Diagnol Pitch (mils)=	17.9605	Diameter(mils)=	6
Total MOSFET Width (meters)=	12.5	% 4x4 die area=	87.50%

Resistance Component	Symbol	Key Parameter	Parameter Units			Source	Portion	Drain	Portion	Total (S+D)	Resistance Ohms	Resistance Micro-ohms	Integrated Resistance Micro-ohms	Explanation Conservative Nominal Difference
Silicon/Translator														
Channel	Rch	580	Ω-µm	at Vgs(V)=	2.5	Rch/2 =	0.0000232	Rch/2 =	0.0000232	Rch=	0.0000464	46.4	46.4	-
Source, Drain	Rs, Rd	190	Ω-µm			Rs =	0.0000152	Rd=	0.0000152	Rs + Rd=	0.0000304	30.4	76.8	-
On-Chip Metallization														
S/D Silicide (Mo)	R(Mo)	4	Ω/Sq	0.375	µm	RSMo=	0.00000012	RDMo=	0.00000012	Rs+d(Mo)=	0.00000024	0.24	77.04	-
Silicide-M1 Via	RV01	7.5	Ω/Cut	12500000	Cuts	RV01s=	0.0000006	RV01d=	0.0000006	RV01s+d=	0.0000012	1.2	78.24	-
M1 Stripe (S,D)	RM1	0.08	Ω/Sq	250000	16.66666667	RM1s=	2.66667E-06	RM1d=	2.66667E-06	RM1s+d=	5.33333E-06	5.333333333	83.57333333	Only half of the S or D currer
M1-M2 Via (S,D)	RV12	5	Ω/Cut	6250000	Cuts	RV12s=	0.0000008	RV12d=	0.0000008	RV12s+d=	0.0000016	1.6	85.17333333	
M2 S, D Stripe	RM2	0.08	Ω/Sq			RM2s=	0	RM2d=	0.000001	RM2s+d=	0.000001	1	86.17333333	x1.5 is for Diagonal drain pat
M2-M3 Via (S)	RV23s	5	Ω/Cut	25000000	Cuts	RV23s=	0.0000002			RV23s=	0.0000002	0.2	86.37333333	Could Actually Get in 2x mor
M2-M3 Via (D)	RV23d	5	Ω/Cut	150000	Patches	3750000		RV23d=	1.33333E-06	RV23d=	1.33333E-06	1.333333333	87.70666667	
M3-M4 Via (D)	RV 34d	5	Ω/Cut	150000	Patches			RV34d=	1.33333E-06	RV34d=	1.33333E-06	1.333333333	89.04	
M3-M4 Via (S)	RV34s	5	Ω/Cut	300000	Patches	RV34s=	6.66667E-07			RV34s=	6.66667E-07	0.666666667	89.70666667	Assume same patch pattern
M4-M5 Via (S)	RV45s	5	Ω/Cut	150000	Patches	RV45s=	1.33333E-06			RV45s=	1.33333E-06	1.333333333	91.04	Straight through to M5 under
M4 Spread to M5 (D)	RM4d	0.0571429	M4|M2 Ω/Sq	0.02352941	128			RM4d=	3.35759E-05	RM4d=	3.35759E-05	33.57593896	124.6159390	Assume 40% area coverage
M3 Spread to M5 (S)	RM3s	0.0571429	M3|M2 Ω/Sq	0.02352941	128	RM3s=	3.35759E-05			RM3s=	3.35759E-05	33.57593896	158.1918679	
M5 Spread to Ball (D)	RM5d	0.0235294	M5|M4|.5M2	0.00260818	128			RM5d=	1.0524E-05	RM5d=	1.0524E-05	10.52397587	168.7158438	
M5 Spread to Ball (S)	RM5s	0.0235294	M5|M3|.5M2	0.00260818	128	RM5s=	1.0524E-05			RM5s=	1.0524E-05	10.52397587	179.2398196	
Package/Interconnect													179.2398196	
Solder Ball Resistamce	RSB	0.0013448	Ω/Ball	128	Balls	RSBs=	1.05042E-05	RSBd=	1.05042E-05	RSBs+d=	2.10085E-05	21.00845249	200.2482721	Diameter=1/2 Ball Pitch, Hei
Drain Pad Resistance	RSBPd	0	Ω/Pad	128	Drain Ball Pads			RSBPd=	0	RSBPd=	0	0	200.2482721	
Worst Source Pad R	RSPwc	0.0067842	Ω/Pad	25%	5.656854249								200.2482721	x1.25 for 4 stud source pad s
Mid Source Pad R	RSPmc	0.0048274	Ω/Pad	50%	4								200.2482721	
Stud Source Pad R	RSPos	0	Ω/Pad	25%	1								200.2482721	
Average Source Pad R	RSPavg	0.0037597	Ω/Pad	128	Source Ball Pads	RSBPs=	2.9373E-05			RSBPs=	2.9373E-05	29.37298491	229.621257	
Source Stud Resistance	Rstud	0.0002367	Ω/Stud	60	Studs	Rstud s=	4.73427E-06			Rstud s=	4.73427E-06	4.734267774	234.3554848	
Drain Thick Copper R	RTCUd	6.693E-05	Ω/Sq	0.625	(Leff)p/Wp			RTCu(d)=	4.18307E-05	RTCu(d)=	4.18307E-05	41.83070866	276.1861935	
Substrate Cu-Invar-Cu	RCICs	3.346E-05	Ω/Sq	0.625		RCICSub(s)=	2.09154E-05			RCICSub(s)=	2.09154E-05	20.91535433	297.1015478	

Total Source+Drain Resistance= 297.1015478 *Micro-Ohms*

FIG. 10